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ART UNIT	PAPER NUMBER
2616	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	04/06/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	09/916,406	KHANKHEL, SAEEDA	
	Examiner	Art Unit	
	Habte Mered	2616	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *1/30/2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-3,5,6,8-15,17-20,22-26 and 28-30* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3,5,6,8-15,17-20,22-26 and 28-30* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on *07-27-2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. The amendment filed on 30 January 2007 has been entered and fully considered.

2. Claims 1-3, 5, 6, 8-15, 17-20, 22-26, and 28-30 are currently pending.

3. Claims 4, 7, 16, 21, and 27 are cancelled.

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. **Claims 1-3, 12, 28 and 29** are rejected under 35 U.S.C. 103(a) as being unpatentable over Huang et al (US 4, 516, 238), hereinafter referred to as Huang, in view of Green et al (US 5, 687, 324), hereinafter referred to as Green.

Huang teaches a full access, non-blocking, wide band switching system in Figure 1 that is designed to switch signals that have destination addresses embedded in the signal structure. The system of Figure 1 comprises of a concentrator, a self-routing sorting network, a trap network, and a self –routing expander.

3. Regarding **claim 1**, Huang discloses a switching system for a telecommunications network **(See Figure 1)**, comprising:

a) a first stage having input and output sides, where the output side is concentrated relative to the input side **(See Column 5, Lines 7-11 and Lines 35-48;Figure 1, element 10)**; and

b) a second stage having input and output sides, where the input side of the second stage is coupled to the output side of the first stage and the output side of the second stage being comprised of a plurality of outputs wherein the second stage is a sort and trap stage that receives a plurality of cells having unique and non-unique destination addresses in a first time slot; **(See Column 5, Lines 10-14; Huang discloses that the first stage (i.e. concentrator) outputs collectively labeled as 1100 in Figure 1 is the input to the second stage and the second stage can be viewed as a stage that includes the sorter sub-network and the optional trap sub-network.)**

Huang, however, fails to teach a trap buffer coupled to the second stage and aging each cell having a non-unique destination address in the trap buffer coupled to the second stage and that the second stage is a non-recirculating sort and trap stage.

Green teaches an ATM switch with multicast capability that uses a feedback mechanism for resolving contentions.

Green discloses aging each cell having a non-unique destination address in the second stage and that the second stage is a non-recirculating sort and trap stage. Green teaches a system wherein the second stage is a non-recirculating sort and trap stage. **(In Figure 2 element 38 is a sorter that can be a Banyan Network. In Figure 2, elements 44 and 46 serve as the trap stage. Therefore, Greene using elements 38, 44 and 46 teaches a non-recirculating sort and trap stage.)** Green further

discloses a plurality of cells arrive at the second stage, in a first time slot, the second stage placing each cell having a unique destination address on a selected one of the plurality of outputs and aging each cell having a non-unique destination address and a buffer **(See Figure 2, element 44 – feedback queue and Column 2, Lines 25-35)** coupled to the second stage **(Collectively in Figure 2, elements 38, 44, and 46 constitute the second stage)** the second stage places each cell having a unique destination address on a selected of one of the plurality of outputs at a next time slot and ages each cell having a non-unique destination address until the destination address becomes unique for a subsequent time slot **(See Column 2, Lines 10-42)** , and discards an aged cell if the destination address does not become unique at a subsequent time slot. **(Green teaches discarding an aged cell form the trap buffer in Column 6: 4-6. Besides the concept of discarding cells/packets when destination is unavailable in the art is well known and Examiner cites US RE34811 to Eng et al. Eng shows in the last paragraph of the description that it is a very well known fact that balancing between storage size and determining the quantity of packets to be discarded is an issue in switching circuits.)**

It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify Huang's switching system to incorporate a non-circulating sort and trap stage architecture to age cells with a non-unique destination address causing output contention. The motivation is to prevent congestion in an efficient manner such that the rate of incoming cells to the sorter stage will not decrease due to

the presence of cells with a non-unique destination address from previous switching cycle as further illustrated in Green's Column 2, Lines 29-31 and Figure 2.

4. Regarding **claim 2**, Huang discloses a switching system wherein the first stage is a concentrator. **(See Element 10 in Figure 1; Column 5, Lines 5-7)**

5. Regarding **claim 3**, Huang discloses a switching system wherein the first stage in Huang's switching system shown in Figure 1 is a concentrator and performs an N: L concentration on cells arriving in the first time slots where N is the number of input connections to the first stage and L is the number of input connections to the second stage. **(See Element 10 in Figure 1; Column 5, Lines 6-11 and Lines 34-52; Huang explains the need for a concentrator and shows why when having N input signals at the concentrator where only L of the non-adjacent N input signals are active at a time the output of the concentrator will be L adjacent active output signals where the non-active input signals are dropped and L < N)**

6. Regarding **claim 12**, Huang discloses a high performance switching system, comprising of a concentrator stage having a plurality of input ports for the switching system and a plurality of outputs, where the concentrator concentrates cells entering the switch on the plurality of input ports and then routes the concentrated cells onto the plurality of outputs by discarding idle ones of the plurality of inputs (**See Huang Column 5, Lines 5-11 and Lines 35-48; See Element 10 in Figure 1).** Huang further discloses that a Batcher-sorter and trap stage having a plurality of inputs and a plurality of outputs, each of the plurality of inputs of the Batcher sorter trap stage coupled to a corresponding one of the plurality of outputs of the concentrator stage and Huang

teaches that a any given cycle or time slot only cells with a unique destination address are sent to the output **(See Huang Column 5, Lines 10-14; Huang discloses that the first stage (i.e. concentrator) outputs collectively labeled as 1100 in Figure 1 is the input to the second stage. The second stage can be viewed as a stage that includes the sorter sub-network and the optional trap sub-network**.)

Huang fails to disclose that the switching system can have a non-re-circulating sorter and trap stage. Huang also fails to disclose that each of the non-re-circulating sorter and trap stage output is coupled to the inputs of a plurality of queues and in turn each output of the plurality of queues is coupled to a corresponding output port and the cells in each queue consist of cells with a common destination address. Huang also fails to disclose that the non-re-circulating sorter and trap stage further comprises a trap buffer in which the selected ones of the plurality of cells arriving thereat during the first one of the plurality of time slots is aged until a next one of the plurality of time slots and discarded if the destination address of said aged cell does not become unique at a subsequent time slot.

Green teaches that an ATM switching system **(See Figure 2)** can have a non-re-circulating sorter and trap stage **(Figure 2, elements 38, 44, and 46)**. Green also discloses that each of the non-re-circulating sorter and trap stage output is coupled to the inputs of a plurality of queues **(Figure 2, element 48 shows a dedicated output queue)** and in turn each output of the plurality of queues is coupled to a corresponding output port **(Figure 2, element 40)** and the cells in each queue consist of cells with a common destination address **(all cells in any given have a common destination**

address – i.e. the specific output port). Green also discloses that the non-re-circulating sorter and trap stage further comprises a trap buffer **(Figure 2, element 44)** in which the selected ones of the plurality of cells arriving thereat during the first one of the plurality of time slots is aged until a next one of the plurality of time slots **(See Column 2, Lines 10-45)** and discarded if the destination address of said aged cell does not become unique at a subsequent time slot. **(Green teaches discarding an aged cell form the trap buffer in Column 6: 4-6. Besides the concept of discarding cells/packets when destination is unavailable in the art is well known and Examiner cites US RE34811 to Eng et al. Eng shows in the last paragraph of the description that it is a very well known fact that balancing between storage size and determining the quantity of packets to be discarded is an issue in switching circuits.)**

It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify Huang's switching system to incorporate a non-re-circulating sorter and trap stage and queuing stage. The motivation to add a non-re-circulating sorter and trap stage is the desire to prevent congestion in an efficient manner such that the rate of incoming cells to the sorter stage will not decrease due to the presence of cells with a non-unique destination address from previous switching cycle as further illustrated in Green's Column 2, Lines 29-31 and Figure 2. The motivation to use a queuing stage stems from the fact that cell switching rate is increased due to output buffer efficiency achieved by using a queuing stage as indicated in Green's Column 2, Lines 43-47.

7. Regarding **claims 28 and 29**, Huang fails to disclose a switching system that comprises a non-re-circulating sort-trap second stage with logic circuitry for: a) wherein the second stage further monitoring the destination addresses of the plurality of cells arriving at the second stage; b) monitoring the destination addresses of the cells in the buffer; and c) placing the cells in the buffer on the selected one of the plurality of outputs if the cell address becomes unique during the next time slot.

Green discloses a switching system that comprises a non-re-circulating sort-trap second stage **(Figure 2, elements 38 and 44)** with logic circuitry for: a) wherein the second stage further monitoring the destination addresses of the plurality of cells arriving at the second stage; b) monitoring the destination addresses of the cells in the buffer; and c) placing the cells in the buffer on the selected one of the plurality of outputs if the cell address becomes unique during the next time slot. **(See Column 2, lines 10-45 and all switching systems have to have a logic circuitry to manage all of its tasks and it is clear from the cited passage that monitoring of the destination addresses of the cells in the trapping buffer as well as all incoming cells has to occur as Green unambiguously discloses that at most one cell can be routed to an output port in a single cell cycle (i.e. time slot) as illustrated in Column 2:27-29)**

It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify Huang's switching system to incorporate a non-re-circulating sorter and trap stage with logic circuitry for: a) wherein the second stage further monitoring the destination addresses of the plurality of cells arriving at the

second stage; b) monitoring the destination addresses of the cells in the buffer; and c) placing the cells in the buffer on the selected one of the plurality of outputs if the cell address becomes unique during the next time slot. The motivation to add a non-re-circulating sorter and trap stage with logic circuitry to monitor destination addresses of cells is the desire to prevent congestion in an efficient manner such that the rate of incoming cells to the sorter stage will not decrease due to the presence of cells with a non-unique destination address from previous switching cycle as further illustrated in Green's Column 2, Lines 29-31 and Figure 2.

8. **Claims 5, 6, 8-11 and 23-26,** are rejected under 35 U.S.C. 103(a) as being unpatentable over Huang in view of Green as applied to claim 1 above, and further in view of Cooperman et al (US 5, 862, 128), hereinafter referred to as Cooperman.

9. Regarding **claims 5 and 8**, the combination of Huang and Green discloses a switching system that has a second stage that comprises a sorter sub-stage for arranging the plurality of cells arriving at the second stage in a first time slot in a first order, where the first order is based upon the destination address. **(See Huang's Column 7, Lines 55-64 and Huang's Column 8, Lines 10-24; It is important to note that the combination of the sorter and trap networks can be viewed as constituting the second stage of Huang's switching system)**

The combination of Huang and Green, as explained in the rejection statement of the parent claim (i.e. claim 1), further discloses a trap substage for placing each cell having a unique destination address on the selected one of the plurality of outputs and

aging each cell having a non-unique destination address **(See Green's Column 2, Lines 25-35)**

The combination of Huang and Green, as explained in the rejection statement of the parent claim (i.e. claim 1), further discloses in the next time slot the trap substage places the aged cells on the plurality of outputs if the non-unique destination address for the aged cells becomes unique in that next time slot **(See Green's Column 2, Lines 32-45)** and discarded if the destination address of said aged cell does not become unique at a subsequent time slot. **(Green teaches discarding an aged cell form the trap buffer in Column 6: 4-6. Besides the concept of discarding cells/packets when destination is unavailable in the art is well known and Examiner cites US RE34811 to Eng et al. Eng shows in the last paragraph of the description that it is a very well known fact that balancing between storage size and determining the quantity of packets to be discarded is an issue in switching circuits.)**

The combination of Huang and Green, however, fails to disclose that the second stage needs to take into consideration the priority assigned to the incoming cells.

Cooperman teaches a system that improves existing switch architecture like that of Huang's by replacing the trap sub-network with a merged buffer architecture that is similar to Green's architecture as shown in Figure 5.

Cooperman teaches that incoming cells are sorted and eventually routed to the appropriate output ports after taking into consideration the destination address and

priority assigned to each of them. **(See Column 3, Lines 1-3 and 49-55; Column 4, Lines 27-32; and Column 5, Lines 8-24)**

It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the combination of Huang's and Green's switching system to incorporate a means and method to sort and route packets or cells based on priority. The motivation to sort and route on priority comes from the fact that a switching system can be an ATM switching system that supports different services with different quality of services (QoS) and priorities and to maintain the contracted QoS the switch has to process and route based on pre-assigned priorities.

10. Regarding **claim 6**, Huang teaches the aforementioned invention, including the sorter sub-stage being a Batcher sorter. **(See Huang Column 7, Lines 65-68)**

11. Regarding **claim 26**, the combination of Huang and Green, as explained in the rejection statement of the parent claim (i.e. claim 1), disclosed the aforementioned invention including a trap buffer in which cells having non-unique destination addresses for the first time are aged until the next time slot. **(See Green's Column 2, Lines 32-45)** The combination of Huang and Green, as explained in the rejection statement of the parent claim (i.e. claim 1), further discloses that the cells in the trap buffer consist of cells with a non-unique destination address. **(See Green's Column 2, Lines 25-45)** The combination of Huang and Green, as explained in the rejection statement of the parent claim (i.e. claim 1), further discloses that each cell passes through the sorter and trap substage only once. **(See Green, Column 2, Lines 25-32)**

12. Regarding **claims 9 and 23**, Huang teaches all aspects of the claimed invention as set forth in the rejection of claim 8 including:

a) a third stage having an input side comprised of a plurality of inputs, each input coupled to a corresponding one of the plurality of outputs of the second stage **(See Huang Column 5, Lines 18-29; Element 40 in Figure 1 and Figures 13-15.)**

b) wherein, in the first time slot and each one of a series of at least one subsequent time slots, the second stage placing a cell having a unique destination address on one of the plurality of outputs **(See Huang Column 3, Lines 45-50 and Column 9, Lines 5-14)**

Huang, however, fails to disclose that the system can be a multi-cast switching system.

19. Regarding **claims 10 and 24**, the combination of Huang and Green and Cooperman disclose all aspects of the claimed invention as set forth in the rejection of claim 9 including that the switch can be a multi-cast switching system **(See Green Column 2, Line 10-13 and Figure 2, element 38)**.

However Huang fails to teach that the third stage of the switch can comprise a queuing stage.

Green teaches an output buffered packet multi-stage switch wherein the switch has a sorter and trap sub-stages **(Figure 2, element 32, 38, 44, and 46)** and the output of the sorter and trap stage is fed to a queuing stage as shown in **Figure 2, element 48**. **(See Column 2, Lines 10-45).**

It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify Huang's switching system by incorporating a queuing stage, the motivation being achieving output buffer efficiency via a queuing stage increases cell switching rate as indicated in Green in Column 2, Lines 43-47.

20. Regarding **claims 11 and 25**, the combination of Huang and Green and Cooperman disclose all aspects of the claimed invention as set forth in the rejection of claim 9 including that the switch can be a multi-cast switching system **(See Green Column 2, Line 10-13 and Figure 2, element 38)**.

Huang fails to disclose that the queuing stage has a plurality of queues that matches the number of outputs of the switching system.

Green discloses that the queuing stage has a plurality of queues that matches the number of outputs of the switching system. Green further teaches an output buffered packet multi-stage switch wherein the queuing stage further comprises a plurality of queues, each having an input coupled to a corresponding one of the plurality of outputs of the second stage and system output; each one of the plurality of queues buffering cells having a common destination address to be output by the switching system. **(See Column 2, Lines 41-47 and Figure 2, elements 40 and 48).**

It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify Huang's switching system by incorporating a queuing stage that has a plurality of queues that matches the number of outputs of the switching system. The motivation being achieving output buffer efficiency via a queuing

stage that has a plurality of queues that matches the number of outputs of the switching system, increases cell switching rate as indicated in Green in Column 2, Lines 43-47.

13. **Claims 13-15** are rejected under 35 U.S.C. 103(a) as being unpatentable over Huang et al (US 4, 516, 238), hereinafter referred to as Huang, in view of Green et al (US 5, 687, 324), hereinafter referred to as Green, as applied to claim 12 above, and further in view of Widjaja et al (US 5, 440, 553), hereinafter referred to as Widjaja.

14. Regarding **claim 13**, the combination of Huang and Green, as explained in the rejection of the parent claim (i.e. claim 12), teaches a switching system that further comprises:

a) a sorter sub-stage for ordering the plurality of cells arriving at the second stage in each one of the plurality of time slots based upon the destination address **(See Huang Column 7, Lines 55-65)** and

b) a trap substage for placing, during each one of the plurality of time slots, each one of the plurality of cells having either a unique destination address on a selected one of the plurality of outputs **(See Huang Column 9, Lines 1-25)**, for each one of the plurality of time slots, the trap substage selecting cells for placement on the plurality of outputs from a set of cells comprised of cells arriving from the sorter substage. **(See Huang Column 5, Lines 14-20)**

d) aging each cell having a non-unique destination address in the second stage and that the second stage is a non-recirculating sort and trap stage and that the cells causing output contention are sent in a different time slot. **(See Green Column 2, Lines 10-45 and Figure 2)**

Huang, however, fails to disclose that the second stage needs to take into consideration the priority assigned to the incoming cells.

Widjaja teaches an output buffered packet switch with flexible buffer management scheme.

Widjaja teaches that incoming cells are sorted and eventually routed to the appropriate output ports after taking into consideration the destination address and priority assigned to each of them. **(See Column 6, Lines 30-35)**

It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify Huang's switching system to incorporate a means and method to sort and route packets or cells based on priority. The motivation to sort and route on priority comes from the fact that a switching system can be an ATM switching system that supports different services with different quality of services (QoS) and priorities and to maintain the contracted QoS the switch has to process and route based on pre-assigned priorities. Widjaja's system is geared to ATM switching architecture as indicated in **Column 2, Lines 5-10**.

15. Regarding **claim 14**, Huang discloses a switching system of wherein the concentrator stage performs N: L concentrations on arriving cells and where N is the number of input connections to the first stage and L is the number of connections to the second stage. **(See Element 10 in Figure 1; Column 5, Lines 6-11 and Lines 34-52; Huang explains the need for a concentrator and shows why when having N input signals at the concentrator where only L of the non-adjacent N input signals are**

active at a time the output of the concentrator will be L adjacent active output signals where the non-active input signals are dropped and L < N)

16. Regarding **claim 15**, Huang discloses a switching system of wherein the sorter sub-stage is a Batcher sorter. **(Column 7, Lines 65-68)**

17. Claims **17, 18, 22, and 30** are rejected under 35 U.S.C. 103(a) as being unpatentable over Huang et al (US 4, 542, 497), hereinafter referred to as A. Huang, in view of Green et al (US 5, 687, 324), hereinafter referred to as Green.

*A. Huang discloses a multi-cast switching system in **Figure 6** that has a broadcast network stage consisting of source sorting sub-stage and copy sub-stage. The source sorting sub-stage, which is element 4 in Figure 6, sorts incoming cells on the source address and feeds it to the copy sub-stage, which is element 42 in Figure 6. Thus, at the outputs of the sorting network, the original cells and the associated empty copy cells with the same source address appear contiguously. The copy sub-stage then replicates the data in each source cell and inserts this data into the data fields of the associated empty copy cells.* **(See A. Huang Column 3, Lines 25-50)**

18. Regarding **claim 17,** the multi-cast switching system disclosed by A. Huang, comprises a broadcast network having input and output sides, the broadcast network receives, on its input side, a plurality of source cells from at least one source and a plurality of empty copy cells, the broadcast network copies data from selected ones of the plurality of source cells and inserts this data in the empty copy cells to produce copies of the source cells **(See A. Huang Column 9, Lines 35-55 and Column 11, Lines 5-10)**

A. Huang discloses that the inputs to the broadcast network consisting of the source sorting and copying sub-stages are source and empty copy cells. A. Huang teaches that the sorting stage is a Batcher stage **(See A. Huang Column 3, Lines 25-50 and Column 9, Lines 35-55)**

A. Huang fails to teach a switching system with a non-circulating sort-trap stage having input and output sides. A. Huang further fails to teach a second stage, i.e. a non-circulating sort-trap stage, wherein a plurality of cells arrive at the second stage, in a first time slot, the second stage placing each cell having a unique destination address on a selected one of the plurality of outputs and aging each cell having a non-unique destination address for the first time slot in a buffer until a next time slot wherein for multicast operation the plurality of cells include source cells and copies of the source cells and the cells in the buffer consist of cells with a non-unique destination address and discards each cell not having a unique destination address in the subsequent time slot.

Green discloses a switching system with a non-circulating sort-trap stage having input and output sides **(See Figure 2, elements 38 and 44)**. Green discloses a second stage, i.e. a non-circulating sort-trap stage, wherein a plurality of cells arrive at the second stage, in a first time slot, the second stage placing each cell having a unique destination address on a selected one of the plurality of outputs and aging each cell having a non-unique destination address for the first time slot in a buffer until a next time slot wherein for multicast operation the plurality of cells include source cells and copies of the source cells and the cells in the buffer consist of cells with a non-unique

destination address **(See Column 2, Lines 10-45)** and discards each cell not having a unique destination address in the subsequent time slot. **(Green teaches discarding an aged cell form the trap buffer in Column 6: 4-6. Besides the concept of discarding cells/packets when destination is unavailable in the art is well known and Examiner cites US RE34811 to Eng et al. Eng shows in the last paragraph of the description that it is a very well known fact that balancing between storage size and determining the quantity of packets to be discarded is an issue in switching circuits.)**

It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify A. Huang's switching system to incorporate a non-circulating sort-trap architecture to age cells causing output contention by having the same destination address in the same time slot. The motivation is to prevent congestion in an efficient manner such that the rate of incoming cells to the sorter stage will not decrease due to the presence of cells with a non-unique destination address from previous switching cycle as further illustrated in Green's Column 2, Lines 29-31 and Figure 2.

19. Regarding **claim 18,** A. Huang discloses a multi-cast switching system wherein the broadcast network further comprises:

a) a source sort stage for sorting source and copy packets entering the source sort stage based upon a data source identifier for each one of the plurality of source packets and the plurality of copy packets **(See Column 10, Lines 57-65)**; and

b) a copy stage for copying data from source packets containing a first data source

identifier to copy packets containing the first data source identifier. **(See Column 11, lines 5-10)**

20. Regarding **claim 30**, A. Huang fails to disclose a multi-cast switching system that comprises a non-re-circulating sort-trap second stage with logic circuitry for: a) wherein the second stage further monitoring the destination addresses of the plurality of cells arriving at the second stage; b) monitoring the destination addresses of the cells in the buffer; and c) placing the cells in the buffer on the selected one of the plurality of outputs if the cell address becomes unique during the next time slot.

Green discloses a multi-cast switching system that comprises a non-re-circulating sort-trap second stage **(Figure 2, elements 38 and 44)** with logic circuitry for: a) wherein the second stage further monitoring the destination addresses of the plurality of cells arriving at the second stage; b) monitoring the destination addresses of the cells in the buffer; and c) placing the cells in the buffer on the selected one of the plurality of outputs if the cell address becomes unique during the next time slot. **(See Column 2, lines 10-45 and all switching systems have to have a logic circuitry to manage all of its tasks and it is clear from the cited passage that monitoring of the destination addresses of the cells in the trapping buffer as well as all incoming cells has to occur as Green unambiguously discloses that at most one cell can be routed to an output port in a single cell cycle (i.e. time slot) as illustrated in Column 2:27-29)**

It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify Huang's switching system to incorporate a non-re-

circulating sorter and trap stage with logic circuitry for: a) wherein the second stage further monitoring the destination addresses of the plurality of cells arriving at the second stage; b) monitoring the destination addresses of the cells in the buffer; and c) placing the cells in the buffer on the selected one of the plurality of outputs if the cell address becomes unique during the next time slot. The motivation to add a non-re-circulating sorter and trap stage with logic circuitry to monitor destination addresses of cells is the desire to prevent congestion in an efficient manner such that the rate of incoming cells to the sorter stage will not decrease due to the presence of cells with a non-unique destination address from previous switching cycle as further illustrated in Green's Column 2, Lines 29-31 and Figure 2.

21. **Claims 19 and 20** are rejected under 35 U.S.C. 103(a) as being unpatentable over A. Huang in view of Green as applied to claim 17 above, and further in view of Cooperman et al (US 5, 862, 128), hereinafter referred to as Cooperman.

22. Regarding **claim 19**, the combination of A. Huang and Green, as explained in the rejection of the parent claim 17, discloses a multi-cast switching system wherein a non-recirculating Batcher sort-trap stage comprises:

a) a sorter for arranging a plurality of cells arriving at the second stage in the first time slot in a first order where the first order is based on destination address for each arriving cell; **(Green Figure 2, element 38; Column 2, Lines 10-45)**

b) a trap sub-stage for placing each cell with unique destination address on a selected output of the plurality of outputs and aging each cell having a non-unique destination address; **(Green Figure 2, element 44, Column 2, Lines 10-45)**

c) wherein, in a next time slot, the trap sub-stage will place the aged cells on selected outputs of the plurality of outputs if the non-unique destination address for the aged cells become unique in that time slot. **(Green, Column 2, Lines 32-40)**

The combination of A. Huang and Green, also fails to disclose that the second stage needs to take into consideration the priority assigned to the incoming cells.

Cooperman teaches that incoming cells are sorted and eventually routed to the appropriate output ports after taking into consideration the destination address and priority assigned to each of them. **(See Column 3, Lines 1-3 and 49-55; Column 4, Lines 27-32; and Column 5, Lines 8-24)**

It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify A. Huang's switching system to incorporate a means and method to sort and route packets or cells based on priority. The motivation to sort and route on priority comes from the fact that a switching system can be an ATM switching system that supports different services with different quality of services (QoS) and priorities and to maintain the contracted QoS the switch has to process and route based on pre-assigned priorities.

23. Regarding **claim 20**, A. Huang discloses a multi-cast switching system wherein the sub-stage is a Batcher sorter. **(See A. Huang Column 10, Line 67)**

24. Regarding **claim 22**, the combination of A.Huang and Green discloses a switching system that has a second stage that comprises a sorter sub-stage for arranging the plurality of cells arriving at the second stage in a first time slot in a first order, where the first order is based upon the destination address. **(See A. Huang's**

Column 7, Lines 55-64 and Huang's Column 8, Lines 10-24; It is important to note that the combination of the sorter and trap networks can be viewed as constituting the second stage of Huang's switching system)

The combination of A. Huang and Green, as explained in the rejection statement of the parent claim (i.e. claim 17), further discloses a trap substage for placing each cell having a unique destination address on the selected one of the plurality of outputs and aging each cell having a non-unique destination address **(See Green's Column 2, Lines 25-35)**

The combination of A. Huang and Green, as explained in the rejection statement of the parent claim (i.e. claim 17), further discloses in the next time slot the trap substage places the aged cells on the plurality of outputs if the non-unique destination address for the aged cells becomes unique in that next time slot **(See Green's Column 2, Lines 32-45)** and discarded if the destination address of said aged cell does not become unique at a subsequent time slot. **(Green teaches discarding an aged cell form the trap buffer in Column 6: 4-6. Besides the concept of discarding cells/packets when destination is unavailable in the art is well known and Examiner cites US RE34811 to Eng et al. Eng shows in the last paragraph of the description that it is a very well known fact that balancing between storage size and determining the quantity of packets to be discarded is an issue in switching circuits.)**

The combination of A. Huang and Green, however, fails to disclose that the second stage needs to take into consideration the priority assigned to the incoming cells.

Cooperman teaches a system that improves existing switch architecture like that of Huang's by replacing the trap sub-network with a merged buffer architecture that is similar to Green's architecture as shown in Figure 5.

Cooperman teaches that incoming cells are sorted and eventually routed to the appropriate output ports after taking into consideration the destination address and priority assigned to each of them. **(See Column 3, Lines 1-3 and 49-55; Column 4, Lines 27-32; and Column 5, Lines 8-24)**

It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the combination of A. Huang's and Green's switching system to incorporate a means and method to sort and route packets or cells based on priority. The motivation to sort and route on priority comes from the fact that a switching system can be an ATM switching system that supports different services with different quality of services (QoS) and priorities and to maintain the contracted QoS the switch has to process and route based on pre-assigned priorities.

Response to Arguments

25. Applicant's arguments filed on 21 August 2006 have been fully considered but they are not persuasive.

26. In the Remarks, in the 3rd paragraph on page 13, Applicant argues that Examiner continues to cite improperly Green in view of Bianchini, Jr et al (US 5, 287, 346) in view

of Hui and Arthurs "A Broadband Packet Switch for Integrated Transport", IEEE, 1987 ("Hui) to reject the independent claims without making new grounds for rejection.

Examiner respectfully disagrees. The current or previous Office Actions never cited Bianchini or Hui. The independent claims are rejected as shown above by combining Huang with Green. Applicant in the After Final amendment attempted to show Green's 1st embodiment mentioned in the background taught away from a non-circulating trapping stage/buffer and cited Bianchini as supporting Applicant's position. Examiner made it clear in the Advisory which was the response to the After Final filed by Applicant that Bianchini in fact supports Green's 1st embodiment by citing Hui's teaching which also teaches a non-circulating trapping stage/buffer. Examiner has made proper rejections and cited prior arts when needed appropriately.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Habte Mered whose telephone number is 571 272 6046. The examiner can normally be reached on Monday to Friday 9:30AM to 5:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Doris H. To can be reached on 571 272 7629. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

3-29-2007
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